V1.1

PG 信号分离卡使用说明书

（PGV-C001）

技术参数

PG 信号分离卡 PGV-C001 可以接收单端集电极开路输出及差分输出编码器信号，输出差分编码器信号，参数配置如下：

- 5V/500mA（最大）电压源；
- 增量式编码器三相 ABZ 差分输入标准接口；
- 三相 ABZ 差分输出接口；
- 信号频率：≤200KHz；
- 信号幅值：5V±20%。

接口说明

接线端口如图 1 所示：

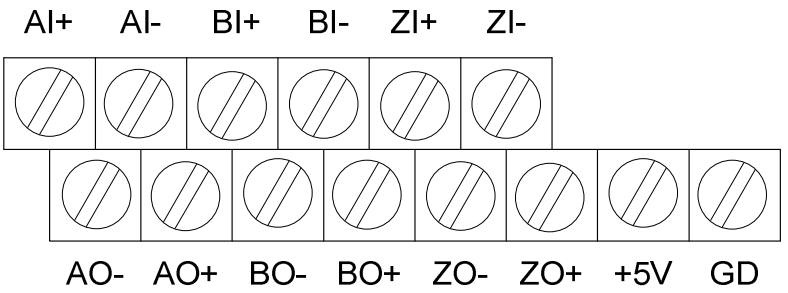

图 1　PG 信号分离卡的端子示意图

端子功能

类型	符号	功能
辅助电源	+5V	向外部提供+5V 最大 500mA 电流
公共端	GD	+5V 电源参考地
差分输出	AO+	编码器 A 相差分（+5V±20%）输出，最大频率≤200 KHz
	AO-	
	BO+	编码器 B 相差分（+5V±20%）输出，最大频率≤200 KHz
	BO-	
	ZO+	编码器 Z 相差分（+5V±20%）输出，最大频率≤200 KHz
	ZO-	
差分输入	AI+	编码器 A 相差分（+5V±20%）输入，最大频率≤200 KHz
	AI-	
	BI+	编码器 B 相差分（+5V±20%）输入，最大频率≤200 KHz
	BI-	
	ZI+	编码器 Z 相差分（+5V±20%）输入，最大频率≤200 KHz
	ZI-	

内部等效电路

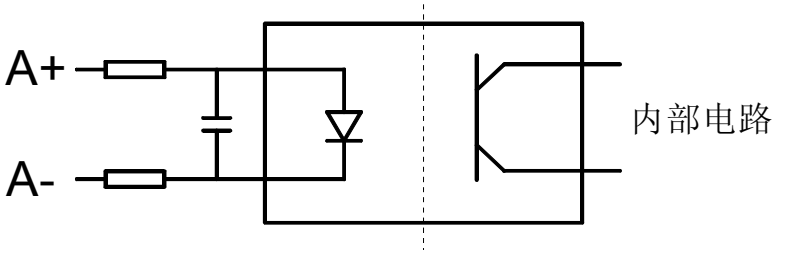

图 2　A 相内部结构等效图

应用连接

以 A 相信号输入为例：

1. 集电极开路输入信号（最大连线长度 50m）。

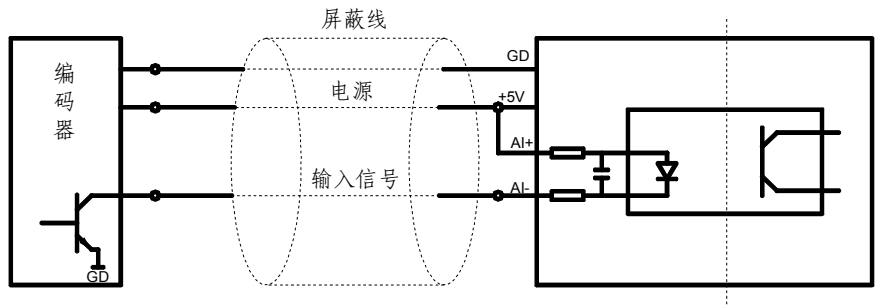

图 3　集电极开路输出图

2. 长线差分驱动输入（最大连接长度 1km）。

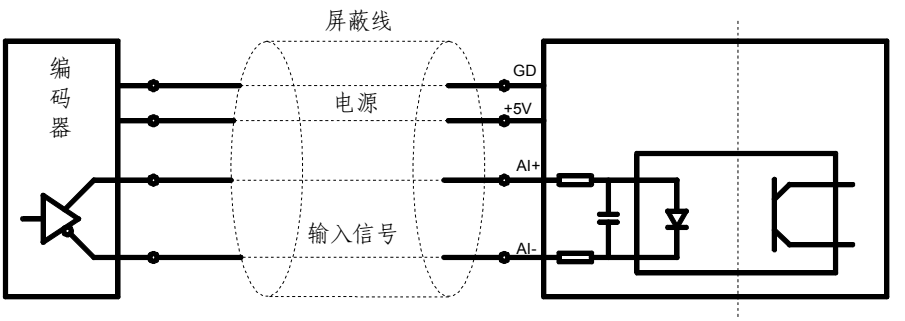

图 4　长线差分输出图

3. 输出信号只适合差分输出，电路连接图见图 4。

注意事项

- 请将信号线与动力线分开布置，禁止平行走线。
- 请务必使用屏蔽电缆作为信号线。
- 请将屏蔽线的屏蔽层单端接大地（如变频器的 E 端）。

USER MANNAL FOR PG SIGNAL ISOLATION CARD

(PGV-C001)

Technical Parameter

PG signal isolation card PGV-C001 could receive single ended open collector output signals and differential output encoder signals, and output differential encoder signals, with following parameter configurations:

- 5V/500mA (maximum) voltage supply;
- Incremental encoder three-phase ABZ differential input standard interface;
- Three-phase ABZ differential output interface;
- Signal frequency: ≤200KHz;
- Signal amplitude value: 5V±20%.

Interface

Wiring terminals are shown in Figure 1:

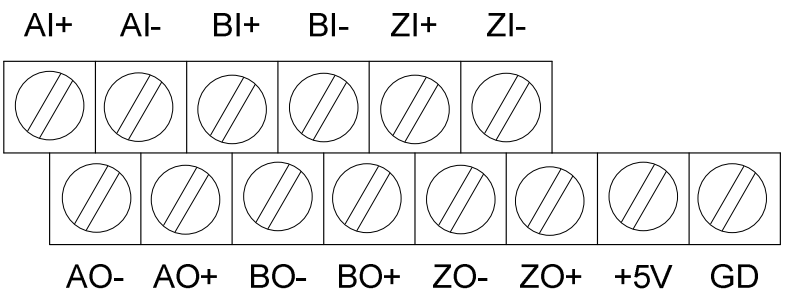

Figure 1 Diagram of Terminals of PG Signal Isolation Card

Terminals Specification

Type	Symbol	Function
Auxilliary power	+5V	Providing +5V maximum 500mA current externally
Common terminal	GD	+5V power reference ground
Differential Output	AO+	Encoder A-phase differential (+5V±20%) output, maximum frequency ≤200 KHz
	AO-	
	BO+	Encoder B-phase differential (+5V±20%) output, maximum frequency ≤200 KHz
	BO-	
	ZO+	Encoder Z-phase differential (+5V±20%) output, maximum frequency ≤200 KHz
	ZO-	
Differential input	AI+	Encoder A-phase differential (+5V±20%) input, maximum frequency ≤200 KHz
	AI-	
	BI+	Encoder B-phase differential (+5V±20%) input, maximum frequency ≤200 KHz
	BI-	
	ZI+	Encoder Z-phase differential (+5V±20%) input, maximum frequency ≤200 KHz
	ZI-	

Internal Equivalent Diagram

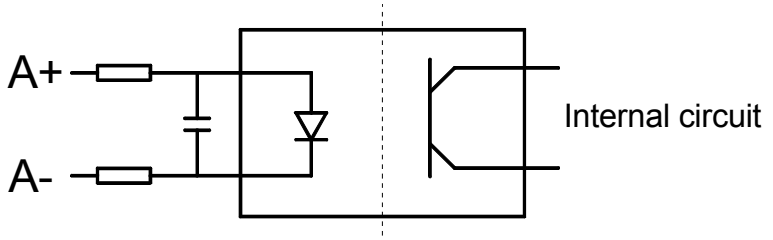

Figure 2 A-phase Internal Structure Equivalent Diagram

Application Connection

Taking A signal input as example:

1. Open collector input signal (wire length$_{(max)}$=50m).

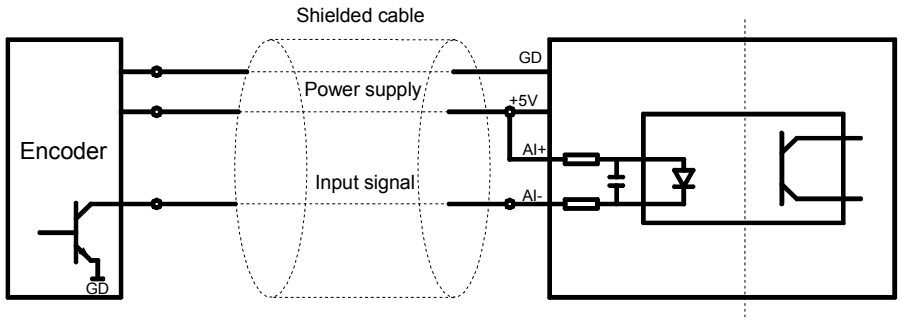

Figure 3 Open Collector Output Diagram

2. Long line differential drive input (wire length$_{(max)}$=1km).

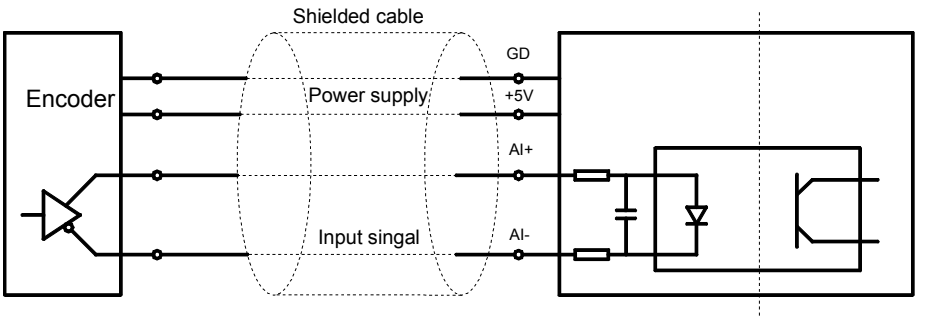

Figure 4 Long Line Differential Output Diagram

3. Output signal only applies to differential output. Refer to Figure 4 for circuit.

Precaution

- Signal line and power line should be laid separately, but should not be paralleled.
- Make sure using shielded cable as signal line.
- Shielding layer of the shielded cable should be grounded at single end (such as E end of frequency converter).